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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/810,905
Filing Date: March 26, 2004
Appellant(s): BU ET AL.

Rose Alyssa Keagy
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/14/2009 appealing from the Office action mailed 5/26/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The divisional case, US Patent Application serial number 11/372,430 filed 3-09-2006 was appealed. The BPAI affirmed the Examiner's final rejections of Claims 11-18 in its decision dated 6-24-2009. The case was subsequently abandoned. In accordance with 37 C.F.R. 41.37(c) (1) (ii) and 37 C.F.R. 41.37(c) (1) (x), a copy of the decision dated 6-24-2009 is included in the appeal brief filed 12/14/2009; the section titled Related Proceedings Appendix.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 6,037,639 A	Ahmad; Aftab	3-2000
US 20050136583 A1	Chen, Chien-Hao et al.	6-2005
US 20040061228 A1	Wieczorek, Karsten et al.	4-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad (US 6,037,639) in view of Chen et al. (2005/0136583 A1).

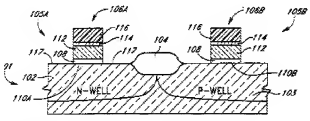

Fig. 1

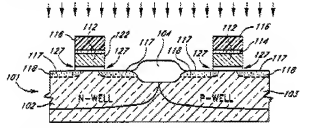

Fig. 2

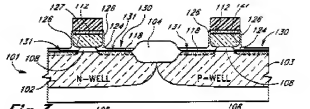

Fig. 3

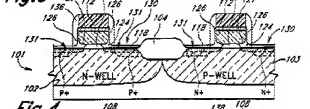

Fig. 4

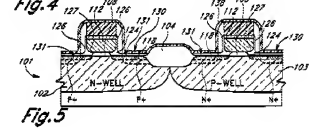

Fig. 5

Regarding claim 1, Ahmad discloses a method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Fig. 1)

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Ahmad, Fig. 2);

depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (Ahmad, Fig. 4 –[136] – silicon oxide layer [136] is

deposited on silicon oxide layer [130] forming a silicon oxide a single silicon oxide layer which is in contact with the "total exposed surface." *NOTE: Alternatively the grown silicon oxide layer [130] is capable of being "deposited" as opposed to grown and thereby be considered the said insulating material. Growing is a widely accepted functional equivalent to "depositing" when forming silicon oxide layers. It is noted that Ahmad discloses forming silicon oxide layers by both process through out the disclosure, therefore it would be obvious to one of ordinary skill in the art to select one of the known conventional methods of forming SiO2 when forming a SiO2 layer. Depositing or growing is merely matter of obvious design choice);*

forming an interfacial layer of nitrogen below the layer of insulating material within the total exposed surface of the lightly-doped extension regions (Ahmad, Figs. 3 and 4, Col. 1 line 66 to Col. 2 lin 11 and/or Col. 2 lines 44-61 – Figure *for depicts the interfacial layer "below" the insulating material [136]*);

forming at least one sidewall layer coupled to the layer of insulating material (Ahmad, Fig. 4 –[126]);

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Ahmad, Fig. 4);

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Ahmad, Fig. 5 - [138]).

Annealing is a implicitly understood step that it is required in order activate the dopants.

Ahmad is however silent upon explicitly annealing, after the formation of the capping layer and with the capping layer in place, then removing all of the capping layer after the annealing.

This sequence of steps was however conventionally known to one of ordinary skill in the art at the time of the invention.

At the time of the invention it was known in that the induced strain/stress in the channel region of a CMOS device can be modified by performing the annealing step with the capping layer in place. This known processing sequence when forming a CMOS device is disclosed by Chen et al. Chen discloses the sequence of steps comprising:

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Chen, Fig. 3 - [24]);

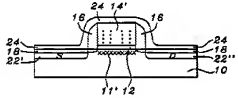

FIG. 3

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions (Chen, Fig. 4 - [27] paragraph [0051]); and

and then teaches that the capping layer is capable of being removed after the annealing (Chen, Fig. 5 - [27] paragraph [0059]);

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Ahmad and Chen to enable the CMOS production step of Chen to be performed according to the teachings of Chen because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed CMOS production step of Chen and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

NOTE: Chen et al. discloses all of the claimed limitations except for the step of implanting a interfacial layer of nitrogen. Additionally, it would be obvious to one of ordinary skill in the art at the time of the invention, in view of Ahmad, to perform an additional step of forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, merely to achieve the benefits associated to the silicide formation as disclosed by Wieczorek.

Claims 2–10 and 19 -20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad in view of Chen et al. in further view of Wieczorek et al (US 2004/0061228 A1).

Regarding claims 2-3, Ahmad in view of Chen disclose the method of claim 1. Ahmad is however silent upon the desired dopant concentration for the source and drain regions. It would however to obvious to one of ordinary skill in the art to be capable of selecting the proper doping concentration from conventionally known ranges

to meet the desired design/operating parameters of the device being manufactured. For a supporting example of one of ordinary skill in the art disclosing the claimed convention doping concentration range see Wieczorek, paragraph [0034]. Wieczorek disclosed wherein the extension, source, and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the dopant concentration through routine experimentation and optimization to obtain optimal or desired device performance because the dopant concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 4, Ahmad in view of Chen disclose the method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (Ahmad, Col. 4 lines 8-15).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the nitrogen concentration through routine experimentation and optimization to obtain optimal or desired device performance because the nitrogen concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

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An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 5, Ahmad in view of Chen disclose the method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide (Ahmad, Fig. 3 –[126], Col. 1 line 66 to Col. 2 lin 11 and/or Col. 2 lines 44-61);

Regarding claim 6, Ahmad in view of Chen disclose the method of claim 1 wherein the step of forming an interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH3 thermal annealing, an NH3 or N2 plasma treatment, or an N implantation (Ahmad, Fig. 3 –[126], Col. 1 line 66 to Col. 2 lin 11 and/or Col. 2 lines 44-61);

Regarding claim 7, Ahmad in view of Chen disclose the method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms (Chen, paragraph [0048], Ahmad discloses the capping layer however is silent upon the thickness).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the thickness through routine experimentation and optimization to obtain optimal or desired device performance because the thickness is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has

been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Regarding claim 8, Ahmad in view of Chen disclose the method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (Chen, paragraph [0051] RTA will be below 10 seconds).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the temperature through routine experimentation and optimization to obtain optimal or desired device performance because the temperature is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Regarding claim 9, Ahmad in view of Chen disclose the method of claim 1 wherein the step of forming at least one sidewall layer includes the use of a BTBAS precursor (Chen, paragraph [0046]).

Regarding claim 10, Ahmad discloses a method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Fig. 1)

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Ahmad, Fig. 2);

depositing a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (Ahmad, Fig. 4 –[136] – silicon oxide layer [136] is deposited on silicon oxide layer [130] forming a silicon oxide a single silicon oxide layer which is in contact with the "total exposed surface." *NOTE: Alternatively the grown silicon oxide layer [130] is capable of being "deposited" as opposed to grown and thereby be considered the said insulating material. Growing is a widely accepted functional equivalent to "depositing" when forming silicon oxide layers. It is noted that Ahmad discloses forming silicon oxide layers by both process through out the disclosure, therefore it would be obvious to one of ordinary skill in the art to select one of the known conventional methods of forming SiO2 when forming a SiO2 layer. Depositing or growing is merely matter of obvious design choice*);

forming an interfacial layer of nitrogen below the layer of insulating material within the total exposed surface of the lightly-doped extension regions (Ahmad, Figs. 3

and 4, Col. 1 line 66 to Col. 2 lin 11 and/or Col. 2 lines 44-61 – Figure *for depicts the interfacial layer "below" the insulating material [136]*);

forming at least one sidewall layer coupled to the layer of insulating material (Ahmad, Fig. 4 –[126]);

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Ahmad, Fig. 4);

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Ahmad, Fig. 5 - [138]).

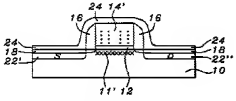
Annealing is a implicitly understood step that is required in order activate the dopants.

Ahmad is however silent upon explicitly annealing, after the formation of the capping layer and with the capping layer in place, then removing all of the capping layer after the annealing.

This sequence of steps was however conventionally known to one of ordinary skill in the art at the time of the invention.

At the time of the invention it was known in that the induced strain/stress in the channel region of a CMOS device can be modified by performing the annealing step with the capping layer in place. This known processing sequence when forming a CMOS device is disclosed by Chen et al. Chen discloses the sequence of steps comprising:

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Chen, Fig. 3 - [24]);



FIC. 3

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions (Chen, Fig. 4 - [27] paragraph [0051]); and

and then teaches that the capping layer is capable of being removed after the annealing (Chen, Fig. 5 - [27] paragraph [0059]);

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Ahmad and Chen to enable the CMOS production step of Chen to be performed according to the teachings of Chen because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed CMOS production step of Chen and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (Ahmad, Col. 4 lines 8-15).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the nitrogen concentration through routine experimentation and optimization to obtain optimal or

desired device performance because the nitrogen concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

wherein the capping layer has a thickness in the range of 200-1000 angstroms (Chen, paragraph [0048], Ahmad discloses the capping layer however is silent upon the thickness).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the thickness through routine experimentation and optimization to obtain optimal or desired device performance because the thickness is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (Chen, paragraph [0051] RTA will be below 10 seconds).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the temperature through routine experimentation and optimization to obtain optimal or desired device performance because the temperature is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Ahmad is silent upon the desired dopant concentration for the source and drain regions. It would however to obvious to one of ordinary skill in the art to be capable of selecting the proper doping concentration from conventionally known ranges to meet the desired design/operating parameters of the device being manufactured. For a supporting example of one of ordinary skill in the art disclosing the claimed convention doping concentration range see Wieczorek, paragraph [0034]. Wieczorek disclosed wherein the extension, source, and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the dopant concentration through routine experimentation and optimization to obtain optimal or desired device performance because the dopant concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any

unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Regarding claims 19 and 20, the prior art references Wieczorek and Chen are silent upon the step of breaking vacuum during the processing, therefore the Examiner take the position the prior art does not teach "breaking vacuum" thus the process is understood to be performed without breaking vacuum.

(10) Response to Argument

Appellant's arguments filed 12/14/2009 have been fully considered but they are not persuasive.

It is first noted that there appears to be confusion regarding the prior art device as disclosed and depicted by Ahmad. The figures depicted in Ahmad are disclosed to implicitly comprise addition conventionally known features which are omitted from the drawings. For example the LDD regions are not depicted but however disclosed to be present and understood to be formed at the time of the process depicted in figure 2. The relevant paragraphs from the Ahmad reference are provided below (Col. 3 line 48-Col. 4 line 7).

> 5) Referring now to FIG. 2, the in-process CMOS circuitry 100 of FIG. 1 is subjected to an ion implantation process with ion dopants selected from a suitable species which can form a preselected silicon-based insulator when reacted with silicon. This ion implantation process forms an ion implanted area 118 in source/drain regions 117 and also in the exposed portions of the substrate 103 (not shown). In the preferred embodiment, the implanted ions are nitrogen ions and the preselected silicon-based insulator is nitride which is formed in the manner explained below. In particular, ion implantation forms a specific concentration and distribution of dopant atoms in the ion implanted areas 118 of the substrate 101. In fact, the implantation process alters the ordered substrate crystal structure and distorts the crystal lattice to accommodate these extra atoms in the implantation area 118.
>
> (6) This type of transformation is called amorphization which is, in this embodiment, caused by nitrogen implant atoms. However, as will be fully understood in the next process step, these amorphous implant areas 118 are advantageously used as a nitrogen atom source during the formation of a nitride insulating layer along the side walls 122 of the gate structures 106A, 106B. Additionally, amorphization of the silicon substrate by implanting nitrogen prevents the out diffusion of LDD implants (As, P, etc.) which reduces the need for the conventional Si or Ge deposition step used to prevent this out diffusion in the prior art.

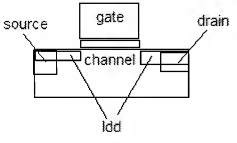
Claim 1, 10:

Appellants traverse the rejection of the claims with the argument that "element 118 of FIG. 2 is the amorphous ion implant area (Column 3 lines 48-67), but not an implantation of arsenic or phosphorous that is needed for the lightly-doped extension regions (column 3 lines 36-41)."

In response, element 118 was not indicated in the rejection to be a LDD region. Ahmad explicitly discloses that LDD (LDD is synonymous with lightly doped extension) regions are present in the device depicted in figure 2 but are not however shown in the figures (Col. 3, lines 37-47). Element 118 is disclosed in the Ahmad reference to be the

implanted nitrogen ions which are analogous to the interfacial layer of nitrogen as claimed.

The required location of the LDD regions is implicitly understood to an artesian. A conventional is a sub-structure in a MOSFETT that is intended to permit operation with higher drain-source voltage and is located between the source-drain and the channel region. For clarity a drawing by the examiner illustrating the implicit location of a LDD region in a MOSFET is provided below.



It is noted that if Ahmad had drawn the LDD regions, it is understood that the LDD regions would appear in figure 2 substantially overlapping with the impurity region 118 possibly confusing the figure.

As demonstrated in figures 3-5, a insulative material is deposited/grown upon the exposed surface of figure 2 which is disclosed to have the claimed LDD region even though not explicitly shown. It is implicitly understood from what is known in the art regarding LDD regions that the depicted insulation layer of figures 3-5 is clearly over and contacting exposed LDD region of figure 2.

Regarding the argument that Ahmad teaches growing the insulation layer (SiO2) rather than depositing (SiO2). This argument is traversed because the methods of growing and depositing when describing the formation of a SiO2 layer are known functional equivalent methods of forming a SiO2 layer. Throughout the entirety of the reference, Ahmad discloses that SiO2 layers are formed from both deposition and growth. The appellants argue that a growth process caries a the significant penalty of a high thermal budget that lowers the manufacturing yield, however there has been no showing that depositing yields any different results from growing. Therefore the arguments can not be considered persuasive because a *prima facie* case of obviousness under 35 U.S.C. 103(a) has been established, therefore it is the bourdon to the Appellants to provide objective evidence which must be factually supported, for example by an appropriate affidavit or declaration. It is further noted the arguments of counsel cannot take the place of evidence in the record.

Regarding the argument that Ahmad does not teach the interfacial layer of nitrogen, element 118 as addressed *supra* is implanted nitrogen ions. These nitrogen ions are disclosed to be present at the interface between the insulating layer and the substrate where the ions were disclosed to be implanted. (NOTE: It is understood in the art that the LDD (A.K.A: Lightly Dope ***Drain***) is part of the source/drain regions.) As disclosed in col. 4 lines 44-51, nitrogen atoms migrate up to the insulating layer at the substrate surface, thus explicitly teaching the claimed nitrogen interface.

Regarding the argument that the reference Ahmad does not teach a sidewall coupled to the insulating layer, this feature is explicitly shown in figure 4. Figure 4

explicitly depicts the formation of a SiO2 sidewall [136] formed on the SiO2 insulating layer.

Regarding the argument that the secondary reference Chen does not remove "all" of the SiN capping layer, the reference is merely applied to demonstrate the known convention of removing the capping layer where not needed after it has served its function. Note that that the cited paragraph [0021] merely state that the SiN layer "can" remain on portions of the substrate where it can double as a silicide mask. This step is only discloses as an option an there for not required. From the disclosure, should one of ordinary skill not desire forming silicide contacts, the artesian would be expected to omit leaving a portion of the SiN capping layer and just remove the entire layer.

Furthermore this argument is irrelevant to the rejection as presented, the prior art reference Chen is merely applied to show that a SiN capping layer, which provides the same function, is known to be capable of being removed after it serves its function.

The appellants do not proved a clear explicit showing of why it would not be obvious to remove the layer as asserted in the presented rejection. The arguments are directed to the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.

Claims 2-4:

The claim does not specify what type of dopant is implanted into the soure/drain and/or extension regions. Taking into consideration the Appelant's original disclosure

implantation of a dopant can either be nitrogen to form a nitrogen interface OR dopant to form either a the source, drain and/or LDDs. When implanting nitrogen ions into a semiconductor material, nitrogen is/can be considered a dopant. As such the cited paragraph teaches 1-2 E20 atoms/cm3 when implanting nitrogen to dope the surface region of a semiconductor substrate. Note that the implanted region is the region where the source, drain, and LDD are located, therefore the source drain and LDD regions are disclosed as having a nitrogen doping concentration of 1-2 E15-20 atoms/cm3.

Claim 5:

The Ahmad reference explicitly states that the insulating layer (depicted in figure 3) formed on the exposed surface (shown in figure 2) is silicon oxide thereby clearly meeting the limitation. See regarding Claim 1 *supra*.

Claim 6

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Furthermore both Ahmad and Wieczorek both explicitly disclose implanting nitrogen. The atomic symbol for nitrogen is **N**, therefore **N** (nitrogen) implantation is explicitly taught.

Claim 7

Chen teaches that a capping layer for the intended function is/was known to be formed within the claimed range to achieve the Appellant's disclosed results.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking reference individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim 8

Chen teaches the cap anneal is done in the temperature range of 1000-1100 C by RTA (rapid thermal anneal). RTA by definition is in a time range considerably less than 10 second.

Furthermore the parameters are not and have not been disclosed to be critical. MPEP § 2144.05

Claim 9

Chen discloses in paragraph [0046] BTBAS precursor is capable of being use to form silicon oxide sidewalls. Paragraph 0042 states:

[0042] B) If a silicon oxide/silicon nitride stack capping layer 24 is formed, ***the silicon oxide layer portion is formed under the following conditions*** (with the silicon nitride layer portion being formed under the conditions noted above for the silicon nitride capping layer 24):

The appellants are incorrect when they state paragraph 0046 refers to the process of forming capping layer 24. As state in paragraph 0042 the conditions for forming a SiN capping layer are described prior to paragraph 0042. As stated in paragraph 0042 paragraph 0046 describes condition relating to the formation of the silicon oxide layer portion (ie.. silicon oxide sidewall). Thus the cited portion discloses the known convention of depositing SiO2 to form gate spacer/sidewalls from a BTBAS precursor.

Claims 19 and 20:

The claims broadly state the negative limitation that a vacuum is not broken. The claim construction fails to establish that a vacuum is even present during the steps. If there is no vacuum then no vacuum can be broken. The cited references are silent upon a vacuum therefore, thus no vacuum broken.

(11) Related Proceeding(s) Appendix

Copies of the court or Board decision(s) identified in the Related Appeals and Interferences section of this examiner's answer are provided in the appeal brief filed 12/14/2009; the section titled Related Proceedings Appendix.

Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jarrett J Stark/

Examiner, Art Unit 2823

Conferees:

/Jarrett J Stark/
Examiner, Art Unit 2823

/Matthew S. Smith/
Supervisory Patent Examiner, Art Unit 2823

/David S Martin/
Review Examiner, TC 2800